In the Claims:

Claims 1-6 and 16-21 are pending.

Claims 16-21 are cancelled herein.

Claims 1-6 remain unchanged.

The status of the claims is as follows:

1. (Original) A method for testing memories with seamless data input/output by interleaving seamless bank commands, comprising the steps of:

transferring data to data input/output (I/O) pins of a memory seamlessly; and

inputting control commands to control pins of the memory seamlessly.

2. (Original) The method as claimed in claim 1, wherein the data transferring step, the data are seamlessly inputted to and outputted from the input/output (I/O) pins of the memory.

3. (Original) The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly inputted into the input/output (I/O) pins of the memory.

4. (Original) The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly outputted from the input/output (I/O) pins of the memory.

5. (Original) The method as claimed in claim 1, wherein the memory has at least two banks that have the control pins for receiving the control commands.

6. (Previously amended) The method as claimed in claim 1, wherein the memory is an SDRAM, DDR-DRAM or Rambus RDRAM.

7. (Previously Cancelled).

8. (Previously Cancelled).

9. (Previously Cancelled).

10. (Previously Cancelled).

11. (Previously Cancelled).

12. (Previously Cancelled).

13. (Previously Cancelled).

14. (Previously Cancelled).

15. (Previously Cancelled).

16. (Currently Cancelled).

17. (Currently Cancelled).

18. (Currently Cancelled).

19. (Currently Cancelled).

20. (Currently Cancelled).

21. (Currently Cancelled).